IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.:	09/941,371
Filing Date:	August 28, 2001
Inventor(s):	Mark Kintis
Group Art Unit:	2634
Examiner Name:	File, Erin M.
Customer No.:	27160
Title:	Phase Modulation Power Spreading Used to reduce RF or Microwave Transmitter Output Power Spur Levels
Confirmation No.:	6016

Applicant's Brief On Appeal

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Table of Contents

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application No.:	09/941,371	)
Filing Date:	August 28, 2001	)
Inventor(s):	Mark Kintis	)
Group Art Unit:	2634	)
Examiner Name:	File, Erin M.	)
Customer No.:	27160	)
Title:	Phase Modulation Power Spreading Used to reduce RF or Microwave Transmitter Output Power Spur Levels	)
Confirmation No.:	6016	)

Applicant's Brief On Appeal

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Real Party In Interest

The real party in interest is Northrop Grumman Corporation by way of an assignment from the inventor, Mark Kintis, to TRW, Inc., recorded on reel/frame 012131/0003, and an assignment from TRW, Inc. to Northrop Grumman Corporation, recorded on reel/frame 013751/0849.

Related Appeals and Interferences

There are no other appeals or interferences known to the Appellant or the Appellant's representative, which are believed to directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status Of Claims

Claims 1 and 28 stand rejected under 35 USC § 103(a) as being unpatentable over Thorson US Patent No. 6,101,225 ("the Thorson patent") in view of Horiguchi et al US Patent No. 6,133,791 ("the Horiguchi et al patent") and Spruit et al US Patent No. 6,549,495 ("the Spruit et al patent"). Claims 2-5, 12, 13, 14, 14, 29, 30 and 32 stand rejected under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi et al and Spruit et al patents and further in view of Underbrink et al US Patent No. 6,754,287 ("the Underbrink et al patent"). Claims 15 and 31 stand rejected under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi et al and Spruit et al patents and further in view of Scott US Patent No. 5,784,403 ("the Scott patent"). Claim 6 stands rejected under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi et al and Spruit et al patents and further in view of Koslov US Patent No. 6,052,701 ("the Koslov patent").

Status Of Amendments

All amendments have been entered. The claims as currently amended are included in Appendix A.

Summary Of Claimed Subject Matter

In general, the present invention relates to a mixer, for example, a two stage mixer, for use in a transmitter application. In order to reduce the power level of out of band spurious output signals or spurs, phase modulation power spreading is used. In particular, each mixer is phase modulated or inverse phase modulated, for example, by a direct sequence phase shift keying (BSK) modulator, to spread the power levels of the spurs over a wider bandwidth instead of concentrating the power levels at single frequencies. The system is easily implemented by phase modulating the first mixer stage with a first psuedorandom number (PN) code and inverse phase modulating the second mixer stage with the same PN code. By utilizing phase modulation, the need for relatively complex and expensive second and third order filters is eliminated to reduce the power level of spurs, such as those spurs resulting from the leakage of the local oscillator in the second mixer stage.

Claims 1-6 and 12-15 relate to a mixer apparatus while claims 28-32 are method claims. Claims 1 and 28 are independent. As discussed in paragraph [0021] of the specification on page 7, Claim 1 recites a mixer 42, as illustrated in Fig. 3.

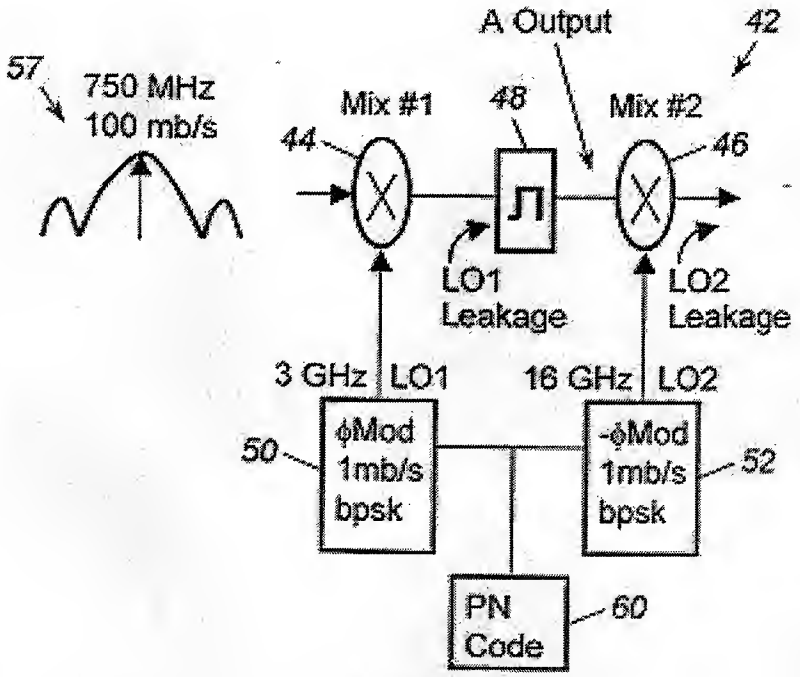

FIG. 3

As discussed on page 7 of the specification in paragraph [0021] , the mixer 42 includes a first mixer stage 44 which includes two input ports recited as"first" and second input ports and a single output port recited as a "first" output port. In the example shown in Fig. 3, a 750 MHz input signal 57 is applied to one of the input ports, e.g. the "first" input port. The other input port, e.g. the "second" input port, is connected to the output of a phase modulator 50. The "first" output port is coupled to an input port, e.g. "third" input port, of a second mixer stage 46. As shown in Fig. 3, a filter 48 may optionally be disposed between the first mixer stage 44 and the second mixer stage 46.

AS discussed in paragraph [0022] on page 7 of the specification, the second mixer stage 46 includes two input ports, recited as a "third" and "fourth" input ports and a single output port

recites as a "second" output port. As mentioned above, one of the "third" or "fourth" input ports are coupled to the "first" output port of the first mixer stage 44. The other input port is connected to an inverse phase modulator 52. The "second" output signal is the output signal of the mixer 42.

Claim 1 includes a phase modulator 50 for modulating a local oscillator signal recited as a "first" local oscillator signal. The "first" local oscillator signal is modulated by a pseudorandom code (PN) 60. As mentioned above, the output of the phase modulator 50 is coupled to one of the "first" or "second" input ports of the first mixer stage 44. This subject matter is discussed on page 7 of the specification.

Claim 1 also includes an inverse phase modulator 52 for inverse phase modulating a local oscillator signal, recited as the "second" local oscillator signal. The "second" local oscillator signal is inverse modulated by the same PN code 60. This subject matter is also discussed on page 7 of the specification.

The dependent claims 2-5 and 7-15 relate to different types of modulators as discussed in paragraph [0025] of the specification. . Dependent Claim 5 relates to the filter 48, illustrated in Fig. 3 above. Independent claim 28 is a method claim which recites the process steps of a mixer as illustrated in Fig. 3 and described in paragraph [0021] of the specification. Claims 29-32 relate to different modulation techniques.

Grounds of Rejection to be Reviewed on Appeal

I. The Examiner's rejection of Claims 1 and 28 under 35 USC § 103(a) as being unpatentable over Thorson, Horiguchi et al and Spruit et al patents.

II. The Examiner's rejection of Claims 2-5, 12, 13, 14, 14, 29, 30 and 32 under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi et al, Spruit et al and Underbrink et al patents.

III. The Examiner's rejection of Claims 15 and 31 under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi et al, Spruit et al patents and the Scott patent.

IV. The Examiner's rejection of 6 under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi et al, Spruit et al and the Koslov patent.

Argument

I. The Examiner's rejection of Claims 1 and 28 under 35 U.S.C. 103(a) as being unpatentable over the Thorson, Horiguchi et al and Spruit et al patents should be reversed.

Claims 1 and 28 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Thorson and Horiguchi et al patents. It is respectfully submitted that the Examiner has failed to set forth a *prima facie* case of obviousness as required by MPEP §2143.

More particularly, § 2143 of the MPEP requires:

> *"To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference, or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. The teaching or suggestion to make the claim combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure."*

As will be discussed in detail below, the rejection fails to meet the criteria of MPEP § 2143 because the references do not disclose all of the elements recited in the claims at issue and a reasonable expectation of success. . In as much as the Examiner has failed to set forth a *prima facie* case of obviousness, it is respectfully submitted that the Examiner's rejection of Claims 1 and 28 must be reversed. .

THE REFERENCES DO NOT DISCLOSE ALL OF THE ELEMENTS

It is respectfully submitted that the reference, namely the Thorson patent and the Horiguchi et al patent, do not disclose all of the limitations of the claims. The Applicant agrees with the Examiner that the Thorson patent fails to disclose modulating a phase modulator modulated with a pseudorandom code and that neither Thorson nor Horiguchi et al disclose an inverse phase modulator which is inverse modulated by the same pseudorandom code as the modulator. It is respectfully submitted that the Examiner's reliance on the Spruit et al patent is misplaced. The Spruit et al patent relates to a device for recording data on an optical disk using a modulation code that is illustrated in Fig. 3a . As set forth in Col. 5, lines 61 and 62 of the Spruit

et al patent, "(d)ata bits are Biphase-encoded." Such a modulation code is not a pseudorandom code. As such, it is respectfully submitted that the Spruit et al patent does not disclose modulation or inverse modulation by way of a pseudorandom code, let alone the ***same*** pseudorandom code. Moreover, none of the references disclose or suggest a two stage mixer in which the output of the first mixer is fed into the input of the second mixer. The Thorson patent actually teaches away from such a configuration. The Board's attention is directed to Fig. 1 of the Thorson patent which illustrates the mixers 120 and 122 whose outputs are connected to a combiner 128. Based on the above, it is respectfully submitted that the Examiner has failed to make out a prima facie case of obviousness for failure to cite references which disclose all of the elements of the claims at issue, contrary to the criteria set forth in the MPEP § 2143

THE EXAMINER HAS FAILED TO SHOW A REASONABLE EXPECTATION OF SUCCESS

The configuration of the two stage mixer, recited in the claims at issue is useful in reducing the power levels of spurious output signals of a mixer. None of the references cited are concerned with the power levels of spurious output signals of a mixer. Moreover, in as much as the references fail to disclose all of the elements of the claims, it is respectfully submitted that no expectation of success of the Examiner's combination can be shown.

For all of the above reasons, it is respectfully submitted that the Examiner has failed to set forth a *prima facie* case of obviousness. Accordingly, the Board is respectfully requested to reverse the Examiner's rejection of Claims 1 and 28.

II The Examiner's rejection of Claims 2-5, 12, 13, 14, 29, 30 and 32 under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi et al, Spruit et al and Underbrink et al patents

Claims 2-5, 12, 13, 14, 29, 30 and 32 stand rejected under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi et al and Spruit et al patents and further in view of the Underbrink et al patent. The Thorson , Horiguchi et al and Spruit et al patents have been discussed above. The Underbrink et al patent was cited for disclosing BPSK modulation. It does not otherwise disclose a two stage mixer as recited in the claims. Claims 2-5, 12, 13, 14, 14, 29,

30 and 32 are dependent claims that are dependent on either Claim 1 or 28. As such, these claims include all of the elements of the independent claims upon which they depend. For these reasons and the above reasons, the Board is respectfully requested to reverse the Examiner's rejection of Claims 2-5, 12, 13, 14, 14, 29, 30 and 32.

III The Examiner's rejection of Claims 15 and 31 under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi et al, Spruit et al and Scott patents

Claims 15 and 31were under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi et al, Spruit et al patents and the Scott patent. The Thorson , Horiguchi et al and Spruit et al patents have been discussed above. The Scott patent was cited for disclosing GMSK modulation. It does not otherwise disclose a two stage mixer as recited in the claims. Claims 15 and 31 are dependent claims that are dependent on Claim 1. As such, these claims include all of the elements of the independent claim 1. For these reasons and the above reasons, the Board is respectfully requested to reverse the Examiner's rejection of Claims 15 and 31.

IV The Examiner's rejection of Claim 6 under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi et al, Spruit et al and Koslov patents

Claim 6 was under 35 USC § 103(a) as being unpatentable over the Thorson, Horiguchi, Spruit et al and the Scott patent. The Thorson , Horiguchi et al and Spruit et al patents have been discussed above. The Koslov patent was cited for disclosing a filter. It does not otherwise disclose a two stage mixer as recited in the claims. Claim 6 is a dependent claim that is dependent on Claim 1. As such, this claim includes all of the elements of the independent claim 1. For these reasons and the above reasons, the Board is respectfully requested to reverse the Examiner's rejection of Claim 6.

Conclusion

It is respectfully submitted that the Examiner's rejection fails to meet all three criteria set forth in § 2143 of the MPEP. First, the Examiner has failed to show that all of the claim elements are disclosed in the cited references. Second, the Examiner has failed to show a reasonable expectation or any expectation of the success of the proposed combination considering the fact that the proposed combination solves a problem of reducing the power level of the spurious output signals of a mixer.None of the references cited even recognize this problem. The Board is respectfully requested to reverse the rejections of all claims by the Examiner.

Respectfully Submitted,

John S. Panaguas
Registration No. 31,051

Date: Dec 28, 2007

KATTEN MUCHIN ROSENMAN LLP
1025 Thomas Jefferson Street, N.W.
East Lobby, Suite 700
Washington, DC 20007-5201
Phone No. (312) 902-5200
Fax No. (312) 902-1061

APPENDIX A
CLAIMS ON APPEAL

1 (Previously Presented) A mixer circuit for reducing the power level of spurious output signals, the mixer comprising:

a first mixer stage which includes a mixer with first and second input ports and an a first output port;

a second mixer stage which includes a second mixer with third and fourth input ports and a second output port, said first input port electrically coupled to one or the other of said third and fourth input ports;

a phase modulator for phase modulating a first local oscillator signal, modulated by a pseudorandom code, said phase modulator electrically coupled to one or the other of said first and second input ports; and

an inverse phase modulator for inverse phase modulating a second local oscillator signal, modulated by the same pseudorandom code as said phase modulator, said inverse phase modulator electrically coupled to the other of said third and fourth input ports.

2. (Original) The mixer circuit as recited in claim 1, wherein said phase modulator is a phase shift keying (PSK) modulator.

3. (Original) The mixer circuit as recited in claim 2, wherein said inverse phase modulator is a phase shift keying (PSK) modulator.

4. (Previously Presented) The mixer circuit as recited in claim 2, wherein said phase modulator is a first direct sequence binary phase shift keying (BPSK) modulator modulated according to a pseudorandom number (PN) code and said mixer circuit includes a PN code generator for generating said PN code.

5. (Original) The mixer circuit as recited in claim 4, wherein said inverse phase modulator is a second direct sequence binary phase shift keying modulator modulated according to said PN code.

6. (Original) The mixer circuit as recited in claim 1, further including an intermediate filter coupled between said first output port and one of said third and fourth input ports.

7. (Canceled) A mixer circuit for reducing the power levels of spurious output signals comprising:

a first mixer having first and second input ports and a first output port; and

a phase modulator for phase modulating a first local oscillator signal, said phase modulator electrically coupled to one or the other of said first and second input ports.

8. (Canceled) The mixer circuit as recited in claim 7, further including a second mixer having third and fourth input ports and a second output port, said first output port electrically connected to one or the other of said third and fourth input ports.

9. (Canceled) The mixer circuit as recited in claim 8, further including an inverse phase modulator, electrically coupled to the other of said third and fourth input ports, said inverse phase modulator configured to inverse phase modulate a second local oscillator signal.

10. (Canceled) The mixer circuit as recited in claim 9, wherein said phase modulator is a direct sequence binary phase shift keying (BPSK) modulator and said mixer circuit includes a psuedorandom number (PN) code generator for generating a PN code for said direct sequence modulation.

11. (Canceled) The mixer circuit as recited in claim 10, wherein said inverse phase modulator is a direct sequence BPSK modulator modulated by said PN code from said PN code sequence generator.

12. (Original) The mixer as recited in claim 1, wherein said modulator and said inverse modulator are configured for QPSK modulation.

13.(Original) The mixer as recited in claim 1, wherein said modulator and said inverse

14.(Original) The mixer as recited in claim 1, wherein said modulator and said inverse modulator are configured for M-ary modulation techniques.

15. (Original) The mixer as recited in claim 1, wherein said modulator and said inverse modulator are configured for GMSK modulation techniques.

16. (Canceled) A mixer circuit for reducing the power levels of spurious output signals comprising:

a first mixer having first and second input ports and a second output port; and

first means for phase modulating a first local oscillator signal applied to one or the other of the first and second input ports.

17. (Canceled) The mixer circuit as recited in claim 16, further including a second mixer circuit having third and forth input ports and a second output port, said first output port connected to one or the other of said third and fourth input ports.

18. (Canceled) The mixer circuit as recited in claim 17, further including second means for phase modulating a second local oscillator signal applied to the other of said third and fourth input ports.

19. (Canceled) The mixer circuit as recited in claim 18, wherein said second phase modulating means is an inverse phase modulator.

20. (Canceled) The mixer circuit as recited in claim 19, wherein said first phase modulating means includes a first phase shift keying (PSK) modulator.

21. (Canceled) The mixer circuit as recited in claim 20, wherein said first PSK modulator is a direct sequence binary PSK (BPSK) modulator and said phase modulating means includes a psuedorandom number (PN) code sequence generator for generating a PN code for modulating said local oscillator signal.

22. (Canceled) The mixer circuit as recited in claim 21, wherein said inverse phase modulator is a direct sequence binary phase shift (BPSK) modulator modulated according to the same PN code as said first means.

23. (Canceled) The mixer as recited in claim 16, wherein said first means includes a first modulation source and the system further includes an inverse modulator for inverse modulating the modulation source.

24. (Canceled) The mixer as recited in claim 18, wherein said first means and second means are configured for QPSK modulation.

25. (Canceled) The mixer as recited in claim 18, wherein said first means and second means are configured for PSK modulation.

26. (Canceled) The mixer as recited in claim 18, wherein said first means and second means are configured for M-ary modulation.

27. (Canceled) The mixer as recited in claim 18, wherein first means and second means are configured for GMSK modulation.

28. (Previously Presented) A method of reducing the power levels of spurious output signals at the output of a mixer circuit comprising the steps of:

(a) providing a two stage mixer including first and second mixer each having a local oscillator port, an input port for receiving first and second local oscillator signals;

(b) phase modulating the first local oscillator signal with a pseudorandom code,; and

(c) inverse phase modulating the second local oscillator signal with the same pseudorandom code used in step (b),.

29. (Original) The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by BPSK modulation techniques.

30. (Original) The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by QPSK modulation techniques.

31. (Original) The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by GMSK modulation techniques.

32. (Original) (The method as recited in claim 28, wherein modulating and inverse modulating in steps (b) and (c) are accomplished by M-ary modulation techniques.

APPENDIX B
EVIDENCE APPENDIX

None

APPENDIX C
RELATED PROCEEDINGS APPENDIX

None